AMENDMENTS TO THE CLAIMS

1. (currently amended) A non-volatile memory comprising:

an array of non-volatile memory cells arranged in a plurality of addressable banks; [[and]]

read/write circuitry coupled to the array, wherein the read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks;

a write latch coupled to the read/write circuitry, wherein the write latch is adapted to store the first data provided on external data communication connections; and

wherein the read and write operations utilize the same set of read/write sense amplifiers.

2. (cancelled)

3. (original) The non-volatile memory of claim 1 wherein the plurality of addressable banks comprise four blocks.

4. (previously presented) The non-volatile memory of claim 1 wherein the read/write circuitry receives the first data from a first external processor, and the read/write circuitry provides the second data in response to one or more second external processors.

5. (previously presented) The non-volatile memory of claim 1 wherein the read/write circuitry writes the first data to an array row of the first one of the plurality of addressable banks and simultaneously reads second data from an array row of each remaining bank of the plurality of addressable banks that is common to the array row of the first one of the plurality of addressable banks.

6. (original) The non-volatile memory of claim 1 wherein the non-volatile memory is a synchronous non-volatile memory.

7. (currently amended) A non-volatile memory comprising:
an array of non-volatile memory cells arranged in a plurality of addressable banks;
a write latch to store first data provided on external data communication connections; [[and]]
read/write circuitry coupled to the array, wherein the read/write circuitry writes the first data to a first one of the plurality of addressable banks and simultaneously reads second data from two or more remaining banks of the plurality of addressable banks; and
wherein the read and write operations utilize the same set of read/write sense amplifiers.

8. (previously presented) The non-volatile memory of claim 7 wherein the read/write circuitry receives the first data from a first external processor, and the read/write circuitry provides the second data in response to one or more second external processors.

9. (currently amended) A processing system comprising:
a processor; and
a non-volatile memory coupled to the processor and comprising,
an array of non-volatile memory cells arranged in a plurality of addressable banks, [[and]]
read/write circuitry coupled to the array, wherein the read/write circuitry writes first data provided by the processor to a first one of the plurality of addressable banks and simultaneously reads second data from two or more

remaining banks of the plurality of addressable banks and provides the second data to the processor,

a write latch, wherein the write latch is adapted to store the first data while it is being written to the first one of the plurality of addressable banks, and

wherein the read and write operations utilize the same set of read/write sense amplifiers.

10. (cancelled)

11. (cancelled)

12. (currently amended) A method of operating a non-volatile memory comprising:

writing first data to a first bank location in a memory array of the non-volatile memory, wherein the first data is stored in a latch circuit prior to writing the first data to the first bank location in the memory array;

substantially simultaneously reading second data from a second bank location in the memory array of the non-volatile memory; [[and]]

substantially simultaneously reading third data from a third bank location in the memory array of the non-volatile memory; and

wherein the read and write operations utilize the same set of read/write sense amplifiers.

13. (original) The method of claim 12 wherein the first data is provided to the non-volatile memory via an external processor.

14. (original) The method of claim 12 wherein the first data is provided to the non-volatile memory via a first external processor, and the method further comprises outputting the second data to a second external processor.

15. (previously presented) The method of claim 12 further comprising accessing a common addressable row of the first, second, and third bank locations prior to writing the first data and reading the second and third data.

16. (cancelled)

17. (currently amended) A method of operating a memory device comprising:
receiving first externally provided data;
storing the first data in a write latch;
writing the first data from the write latch to a first bank location in a memory array of the memory device; [[and]]
substantially simultaneously reading second data from a second bank location in the memory array of the memory device; [[and]]
substantially simultaneously reading third data from a third bank location in the memory array of the memory device; and
wherein the read and write operations utilize the same set of read/write sense amplifiers.

18. (original) The method of claim 17 wherein the first data is provided by an external processor.

19. (previously presented) The method of claim 18 further comprising outputting the second and third data to the external processor.

20. (original) The method of claim 17 wherein the first data is provided by a first external processor, and the method further comprises outputting the second data to a second external processor.

21-30 (cancelled)